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ISO/IEC 14443 higher bit rates with Micore

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Document information

Info	Content
Keywords	Mifare, Micore, ISO/IEC14443, Higher bit rates, Register settings
Abstract	This application describes how to enable and use higher bit rates according to the ISO/IEC14443 using the MF RC530, MF RC531, or the CL RC632.
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Revision history

Rev	Date	Description
01.00	20060413	First initial version
01.01	20060510	Layout correction, Correction of the modulation index in section 4

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1. Introduction

The ISO/IEC14443 offers communication data rates from 106 kbit/s (standard) up to 848 kbit/s. These higher bit rates (212, 424, and 848 kbit/s) are supported by the Micore ICs MF RC531 and CL RC632 (and MF RC530 for ISO/IEC 14443A only). Depending on the contactless smart cards, the bit rates can be different in the uplink (PICC to PCD) and downlink (PCD to PICC). The bit rates have to be selected according to the ISO/IEC14443.

This application note describes how to use the higher bit rates, how to use the Micore ICs with the higher bit rates, and it gives some hints, what has to be considered during the PCD design. So it covers hardware related topics as well as software related ones.

This application note does replace neither any of the ISO/IEC documents nor any of the relevant datasheets.

2. Acronyms and Abbreviations

Table 1: Abbreviations

Table description (optional)

Acronym	Description
HBR	Higher bit rates (data rates of 212, 424 and 848 kbit/s)
PCD	proximity coupling device ("reader")
Micore	Mifare and I-Code reader IC family (here only the MFRC530, MF RC531, and the CL RC632)
PPS	Protocol Parameter Selection
RATS	Request for Answer To Select
ATS	Answer To Select
DS	Divisor Send (PICC to PCD)
DR	Divisor Receive (PCD to PICC)
ATQB	Answer To reQuest type B
RF	Radio Frequency
fc	Carrier frequency (13.56MHz)
Mfout	Signal available at pin 4 of the Micore IC, used for triggering the oscilloscope.

Hexadecimal numbers are noted with a leading "0x".

3. Micore register settings

3.1 ISO/IEC 14443A

3.1.1 Selecting higher bit rates

During the RATS and ATS (see [9]) the PCD and the PICC exchange the necessary parameters for the protocol. In the interface byte TA(1) of the ATS the PICC returns the information whether it supports higher bit rates or not, and if so, which bit rates can be used in which direction.

Table 2: Interface byte TA(1)

	Bit number[1]	Meaning, if set to "1"
	B8	Only the same bit rate in both directions
DS	B7	848 kbit/s supported (PICC to PCD)[2]
	B6	424 kbit/s supported (PICC to PCD)
	B5	212 kbit/s supported (PICC to PCD)
	B4	RFU, must be "0"
DS	B3	848 kbit/s supported (PCD to PICC)
	B2	424 kbit/s supported (PCD to PICC)
	B1	212 kbit/s supported (PCD to PICC)

The PCD shall use the PPS Request to switch to a higher bit rate, using the parameter 1 to request the bit rate. In case no higher bit rates are used, the PPS has to be skipped by the PCD.

Table 3: Parameter 1 of the PPS Request

B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	DSI		DRI	

Table 4: Coding of DSI and DRI

DSI, DRI	11_{bin}	10_{bin}	01_{bin}	00_{bin}
D	8	4	2	1
Bit rate	848 kbit/s	424 kbit/s	212 kbit/s	106 kbit/s

According to the ISO/IEC 14443 the PICC just acknowledges the PPS Request. The following command then is the first command using the selected higher bit rates.

Remark: Sending and Receiving in the means of ISO/IEC 14443 is related to the **PICC,** in this document Sending and Receiving is related to the PCD!

1. Here the bit numbering from bit 1 … bit 8 according to [9] is used.
2. The bit rates are exactly related to the carrier frequency (fc/64, fc/32 and fc/16), so the resulting bit rate e.g. for fc/16 accurately is 847.5kbit/s.

3.1.2 Setting higher bit rates with Micore

Enabling higher bit rates can be done automatically, using the function Mf500PcdSetAttrib in [1]. All the relevant register settings are listed there and in the following tables Table 5: and Table 6:.

Remark: Switching back to the default bit rate can be done with the function Mf500PcdSetDefaultAttrib in [1].

Table 5: ISO/IEC14443A HBR Register Settings PCD to PICC
Micore register settings for sending ISO/IEC14443A HBR

Register Name	Address	106[3]	212	424	848
RegCoderControl	0x14	0x19	0x11	0x09	0x01
RegModWidth	0x15	0x13	0x07	0x03	0x01

Table 6: ISO/IEC14443A HBR Register Settings PICC to PCD
Micore register settings for receiving ISO/IEC14443A HBR

Register Name	Address	106[4]	212	424	848
RegRxControl1	0x19	0x73	0x53	0x33	0x13
RegDecoderControl	0x1A	0x08	0x09	0x09	0x09
RegRxThreshold	0x1C	0x88	0x50	0x50	0x50
RegBPSKDemControl	0x1D	x[5]	0x0C	0x0C	0x0C

Remark: The required speed of the microcontroller should be considered (especially when using frame sizes >64 bytes) as well as the application related limitations regarding the overall transaction time (see chapter 5).

3. This is the default value.
4. This is the default value.
5. Don’t care.

3.2 ISO/IEC 14443B

The activation of higher bit rates according to the ISO/IEC 14443B is described in [8]. In the Protocol Info in the ATQB the PICC returns the Bit_Rate_Capability. The bit rate then is selected in the Param 2 of the ATRIB command. The following command then is the first command using the selected higher bit rates.

For the Micore settings for the communication according to the ISO/IEC 14443B standard bit rate (106 kbit/s) refer to [2] or [3].

Table 7: ISO/IEC14443B HBR Register Settings PCD to PICC
Micore register settings for sending ISO/IEC14443B HBR[6]

Register Name	Address	106	212	424	848
RegCoderControl	0x14	0x20	0x18	0x10	0x08

Table 8: ISO/IEC14443B HBR Register Settings PICC to PCD
Micore register settings for receiving ISO/IEC14443B HBR

Register Name	Address	106	212	424	848
RegRxControl1	0x19	0x73	0x53	0x33	0x13
RegRxThreshold	0x1C	0x88	0x50	0x50	0x50

Remark: The MF RC531 and the CL RC632 were specified and qualified before the ISO/IEC 14443 came up with HBR. The datasheet does not mention it at all. But tests have shown, the MF RC531 and CL RC632 do support the ISO/IEC14443 B higher bit rates.

The use of this Philips IC according to ISO14.443 Type B might infringe third party patent rights. A purchaser of this Philips IC has to take care for appropriate third party patent licenses.

6. This is not specified in the datasheets.

4. PCD Antenna design constraints

There are no specific antenna design constraints for HBR, if the PCD antenna design was done properly according to [4] and [5]. However, it is recommended to check the pulse shapes and the overall performance with HBR against the ISO/IEC 14443 requirements (see chapter 4.1).

It is a physical fact, that higher data rates in general require a higher bandwidth and a higher signal to noise ratio in an RF system, so in some cases it might be more efficient to reduce the quality factor of the PCD antenna to achieve a better communication stability in the field. A lower quality factor also makes the antenna more stable against detuning, which could be caused by environmental changes as well as manufacturing tolerances, and does not necessarily decrease the operating distance. A target quality factor of approximately 21 turns out to be an appropriate value to start with, if not otherwise defined.

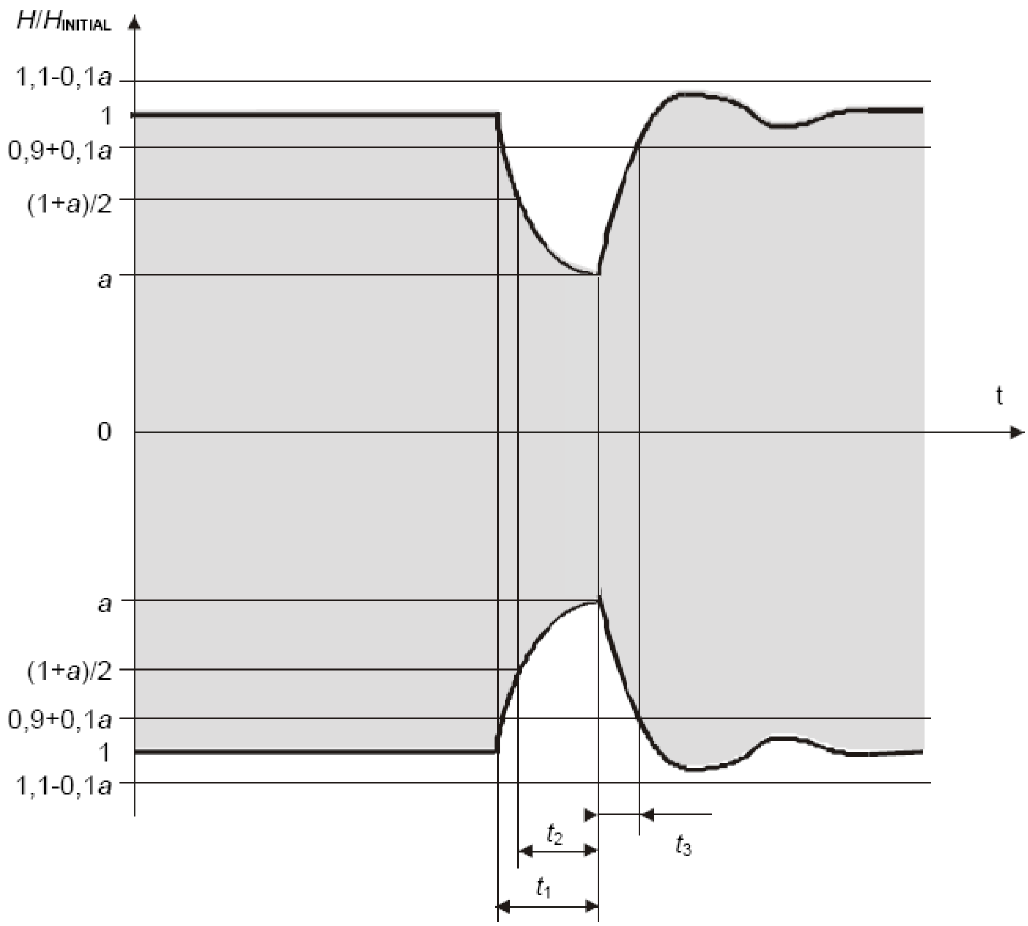
4.1 Tx Pulse shapes for HBR

4.1.1 Basic requirements

The pulse shape requirements for HBR are shown in Fig 1 and Table 10:. According to the ISO/IEC 14443, overshoots shall remain within ± 0,1 x (1-*a*) of $H_{INITIAL}$. The parameter *a* in Fig 1 shall in the range as specified in Table 9: for HBR.

Table 9: Parameter a

Parameter	212 kbit/s		424 kbit/s		848 kbit/s	
	min	max	min	max	min	max
a	0	0,2	0	0,35	0	0,6



(1) Envelope of the carrier

Fig 1. Pulse shape for HBR

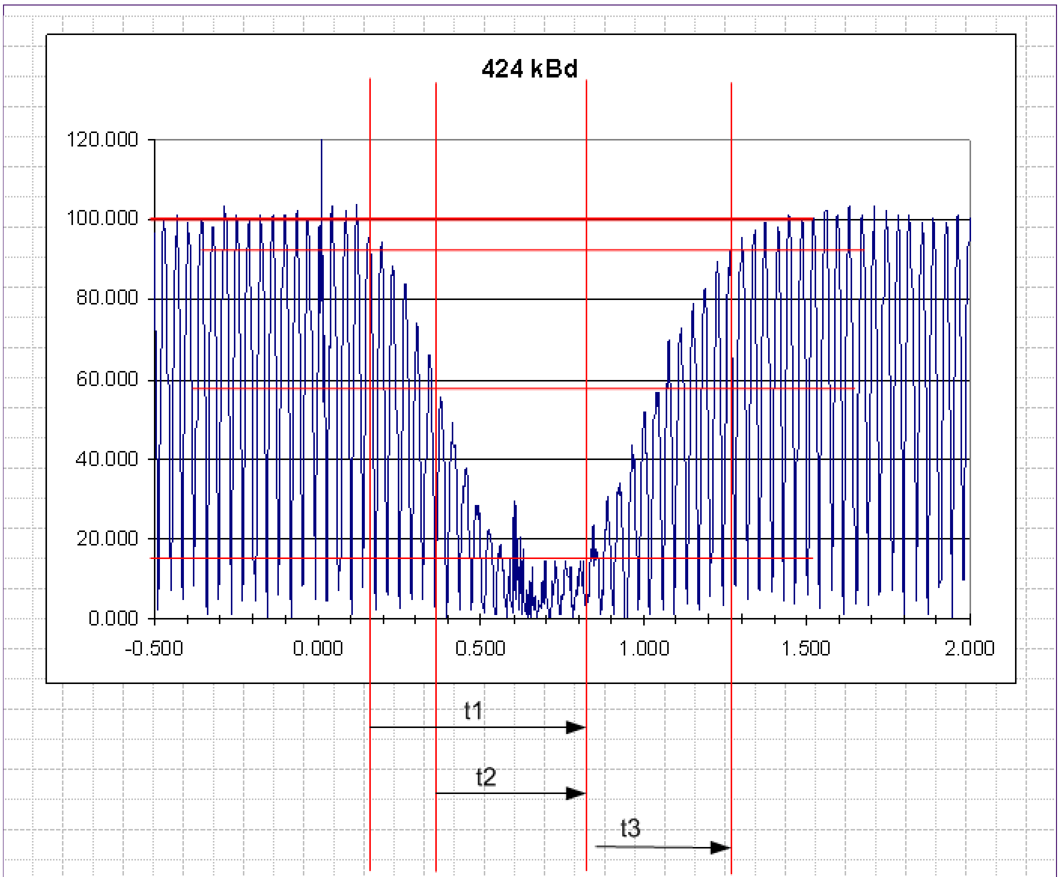
Table 10: Timings of the HBR pulses

Times	212 kbit/s		424 kbit/s		848 kbit/s	
	min	max	min	max	min	max
t_1	15/fc	20/fc	8/fc	10/fc	4/fc	5/fc
t_2	8/fc	t_1	4/fc	t_1	2/fc	t_1
t_3	0	12/fc	0	10/fc	0	8/fc

4.1.2 Measurement example

The following example shows the carrier signal of a PCD, which covers HBR (see Fig 2). The bit rate was switched to 424 kbit/ s and one transmit pulse was measured with an oscilloscope using a Reference-PICC and the Mfout pin of the Micore chip to trigger on the modulation pulse. The spikes at t = 0 and t = 0.6μs, which are related to the trigger signal, shall be ignored in the measurement, because the Mfout pin is not used in the real application, but just for the measurement.

Remark: To get an accurate result, one complete pulse was captured, and the negative half of the signal was multiplied with –1. Thus the signal seems to show a 27 MHz carrier, even though the carrier of course has a frequency of fc = 13.56MHz.



(1) The two spikes are related to the Mfout trigger signal and shall be ignored in the measurement.

Fig 2. Typical pulse shape example for 424 kbit/s

In this example the modulation index can be read as approximately 70%, which is equivalent to $a \approx 17\%$, which gives the points to measure the times t_1, t_2, and t_3:

$$0.9 + 0.1 \cdot a = 0.917$$

$$(1 + a)/2 = 0.585$$

With these values the required times can be calculated and crosschecked with the measurement (read from Fig 2), as shown in Table 11:.

Table 11: Timing example of the HBR pulses

Times	424 kbit/s requirement		424 kbit/s measurement
	min	max	measured
t_1	0.590 μs	0.737μs	0.66 μs
t_2	0.295 μs	0.66 μs	0.46 μs
t_3	0	0.885 μs	0.45 μs

5. The use of higher data rates in applications

Even though the higher bit rates increase the transaction speed, in some cases the standard bit rate might be even more efficient than HBR. To get a better view on the relationship between bit rates and transaction speed, some timing measurements have to be made.

5.1 Transaction speed versus bit rates

So based on the Mifare DESFire card a timing measurement is done, and the overall timing versus bit rate is shown in Table 12: and Fig 3.

Table 12: Transaction time versus bit rate

Mifare DESFire example

bit rate	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Read 1K Byte	130 ms	80 ms	52 ms	43 ms
Read 1k Byte encrypted	171 ms	116 ms	86 ms	76 ms
Read 1k Byte encrypted + PCD time (100ms)	271 ms	216 ms	186 ms	176 ms

This measurement shows the overall time for a read transaction, including the Card activation sequence, protocol activation and card deselection according to the ISO/IEC14443:

REQA, Anticollision, Select[7], RATS, PPS (for switching to HBR), Select Application[8], Read, Deselect

A fast PICC was taken, and just a pure read of data was performed, which reduces the overhead times to a minimum[9]. In addition to that the amount of data was set to 1kbyte to reduce the impact of the card activation sequence (which is always done with 106kbit/s) to a minimum.

Remark: The measurement was done with a DESFire card, which has a frame size of 64 bytes. The HBRs are used with equal bit rates in both directions.

The first example (first line of Table 12:) shows a kind of “best case” scenario: the data is read in plain. This timing is a pure PICC related one, as the command times are measured from transmitting a command until the PICC answer is completely received. So no PCD timing is involved here.

The second example (second line of Table 12:) shows an encrypted read of 1kbyte of data. This timing still is a pure PICC related one, as the command times are measured from transmitting a command until the PICC answer is completely received. So no PCD timing is involved here.

7. The DESFire uses a double size UID, so it requires the Anticollision/Select including cascade level 2.
8. This is a Mifare DESFire related command, and takes appr. 1.5ms (depending on the bit rate)
9. This is the fastest useful application on an ISO/IEC 14443 compliant smart card.

The third example (third line of Table 12:) shows an encrypted read of 1kbyte of data including a PCD timing. The PCD time is assumed to be 100ms, which is quite fast for such a transaction (decryption + data handling, and whatever the system does with the 1kbyte of data).

All three timings are shown in Fig 3.

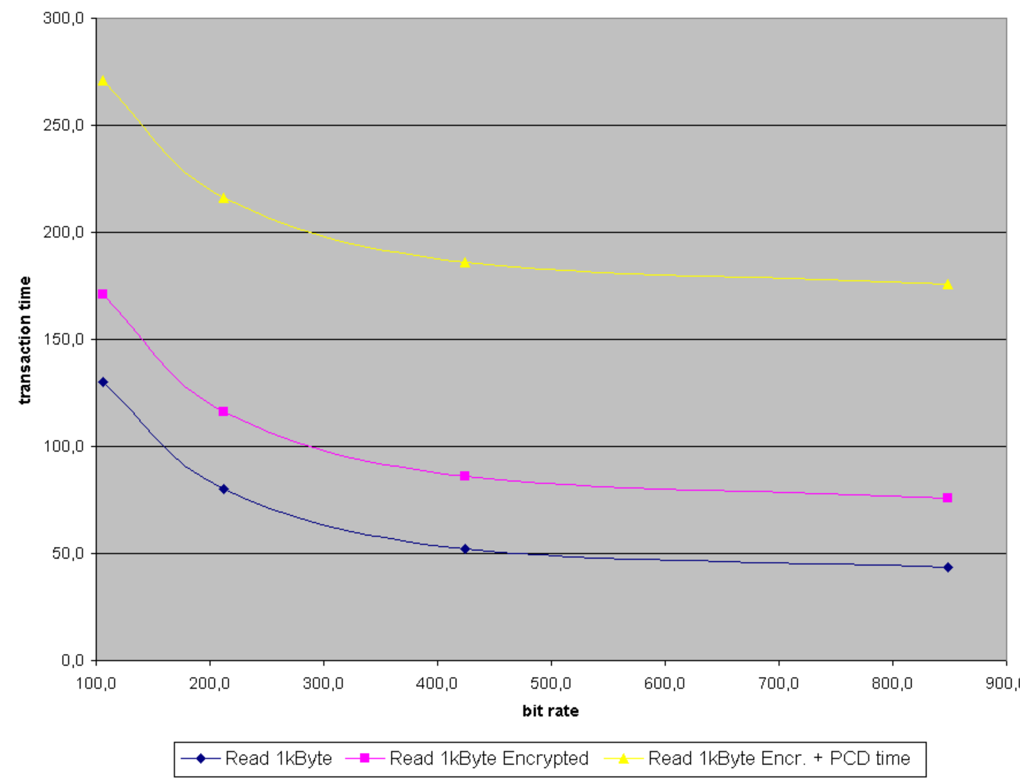


Fig 3. Transaction time versus bit rate (example)

It turns out, that even though this measurement is based on a simple read transaction, the overall transaction time is only partly related to the bit rate. Doubling the bit rate from 106kbit/s to 212kbit/s reduces the transaction from 130ms to 80ms in best case, which gives a “gain” of approximately 40% (see Table 13:).

When doing the same with encryption and considering the PCD – even with a very fast PCD – the result shows, that in a real application, doubling the bit rate from 106kbit/ to 212kbit/s just gives a “gain” of 20%.

The gain is even less, if such an application does not use the “best case” scenario of a pure read, but requires some additional operation on the PICC or in the PCD.

Doubling the bit rate from 424kbit/s to 848kbit/s in such an application only gains 5% (or less) in the overall transaction speed.

Table 13: Gain in transaction speed

	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Read 1K Byte	0	+ 39%	+ 35%	+ 17%
Read 1k Byte encrypted	0	+ 32%	+ 26%	+ 12%
Read 1k Byte encrypted + PCD time (example)	0	+ 20%	+ 14%	+ 5%

5.2 Operating distance versus bit rates

All the previous measurements and calculations have been done without considering the impact of the increasing data rate on the operating distance. In Fig 4 a typical PCD was taken to measure the operating distance versus bit rates. Due to the required higher bandwidth (and so higher signal to noise ratio) the operating distance must decrease at higher bit rates[10]. Here in this example the operating distance decreases from 6.5cm @106kbit/s down to 4cm @848kbit/s.

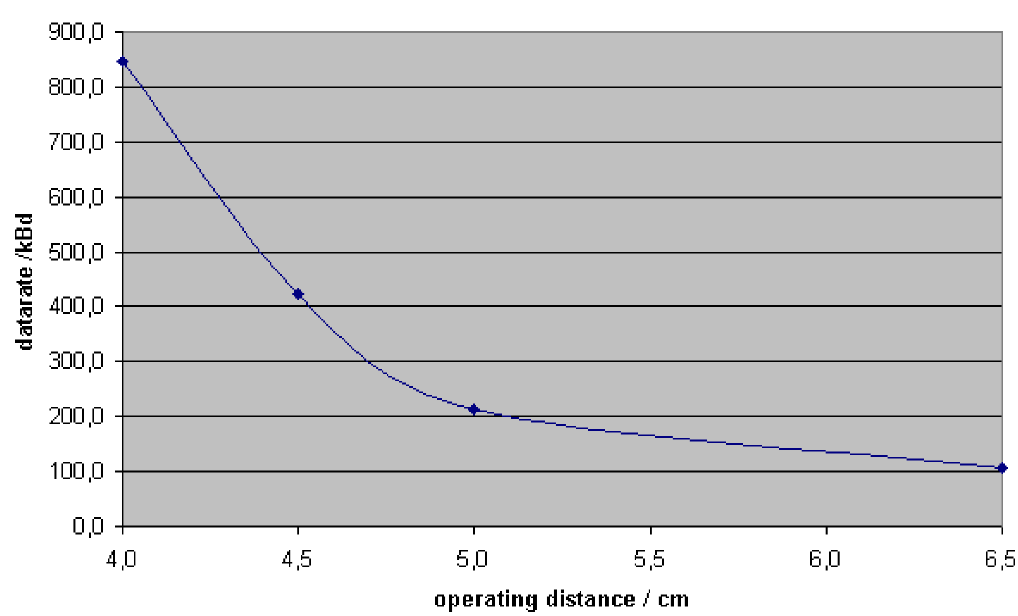


Fig 4. Operating distance versus bit rates (example)

Remark: The given values for the transaction speed and operating distances are just examples.

10. It is not related to the power consumption of the PICC.

6. References

[1] **Software Library -** Sample Source Code, Basic Function Library MF RC5xx

[2] **Functional specification** - MIFARE MF RC531;Highly Integrated ISO 14443 Reader IC; Datasheet

[3] **Functional specification** - Mifare & I-Code CL RC632 Multiple protocol contactless reader IC, Datasheet

[4] **Application note** - MIFARE and I CODE MICORE reader IC family; Directly Matched Antenna Design

[5] **Application note** - Mifare(14443A) 13,56 MHz RFID Proximity Antennas

[6] **ISO/IEC 14443-1**

[7] **ISO/IEC 14443-2**

[8] **ISO/IEC 14443-3**

[9] **ISO/IEC 14443-4**

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